The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A data conversion system comprising:

a first node and a second node in which one of the first node and the second node on an IEEE1394 bus serves as a cycle master, the first node being configured to transmit first data to the second node at a transfer rate synchronized with a cycle start packet output from the cycle master, the second node ~~being~~ having a data conversion unit configured to synchronize second data generated by conversion of the first data in the second node with an external reference signal, the second node to out put the second data,

an external synchronizing signal receiver for receiving the external reference signal provided on at least one of the first and second nodes, and

a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal.

2. (Previously Presented) The data conversion system according to claim 1, wherein

the first data and the second data are image data, and

the first data is a video signal in DV format and the second data is an analog video signal or SDI video signal.

3. (Previously Presented) The data conversion system according to claim 1, wherein the first node serves as cycle master for data transfer.

4. (Previously Presented) The data conversion system according to claim 1, wherein

the second node comprises a second synchronization adjustment unit,

the frequency of the cycle start packet is linked with the frequency of the reference signal by the synchronization adjustment unit of the node that serves as the cycle master.

5 - 7. (Cancelled)

8. (Currently Amended) A device configured to connect to an IEEE1394 bus to form one of a first node and a second node, in a data conversion system in which one of the first node and the second node serves as a cycle master, the first node being configured to transfer a first data to the second node in synchronism with a cycle start packet output from the cycle master on the IEEE1394 bus, the second node being connected on the IEEE1394 bus and being configured to synchronize second data generated by conversion of the first data in the second node with an external reference signal and to output the second data, the device comprising:

an external synchronizing signal receiver for receiving the external reference signal; and

a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using **[[**of**]]** the external reference signal.

9. (Previously Presented) The device according to claim 1, wherein

the first data and the second data are image data, and

the first data is a video signal in DV format and the second data is an analog video signal or SDI video signal.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) The data conversion system according to claim 1, wherein the first node is hardware comprising an 13940HCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as the second data.

14. (Previously Presented) The data conversion system according to claim 1, wherein the second node comprises the external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

15. (Previously Presented) The data conversion system according to claim 1, wherein the first node comprises the synchronization adjustment unit, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit, and the cycle start packet frequency is synchronized with the frequency of the external

reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master.

16. (Previously Presented) The data conversion system according to claim 15, wherein when the first node serves as cycle master, the external reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of an IEEE 1394 interface.

17. (Previously Presented) The data conversion system according to claim 15, comprising a dedicated synchronization signal line for transmitting the external reference signal received by the external synchronizing signal receiver of the second node from the second node to the first node when the first node serves as cycle master.

18. (Previously Presented) The data conversion system according to claim 1, wherein the first node comprises the external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

19. (Currently Amended) The data conversion system according to claim 1, wherein one of the first node and the second node serves **[[and]]** as the cycle master and the other of the first node and the second node includes the synchronization adjustment unit.